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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 10/717,771 | 11/20/2003 | George B. Miller | CSP. 001 | 8373 |

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Robert Gove
CSP Inc.
43 Manning Road
Billerica, MA 01821

| EXAMINER | |
|---|---|
| DILLON, SAMUEL A | |
| **ART UNIT** | **PAPER NUMBER** |
| 2185 | |

DATE MAILED: 04/14/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/717,771 | MILLER, GEORGE B. | |
| | Examiner | Art Unit | |
| | Sam Dillon | 2185 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *20 November 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 November 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

1. The instant application having Application No. 10/717,771 has a total of 18 claims pending in the application; there are 3 independent claims and 15 dependent claims, all of which are ready for examination by the examiner.

## I. INFORMATION CONCERNING OATH/DECLARATION

2. The applicant's oath/declaration has been reviewed by the examiner and is found to conform to the requirements prescribed in 37 C.F.R. ' 1.63.

## II. INFORMATION CONCERNING DRAWINGS

3. The applicant's drawings submitted November 20, 2003 are acceptable for examination purposes.

## III. OBJECTIONS TO THE APPLICATION

4. Claim 9 is objected to because of the following informalities:

a. **Claim 9** reads "and associated **cashe**" on lines 9-10 of page 23, and should be corrected to read "and associated **cache**".

b. **Claim 9** reads "if **the the** system controller" on lines 21-22 of page 23, and should be corrected to read "if **the** system controller".

Appropriate correction is required.

## IV. REJECTIONS BASED ON PRIOR ART

### *Claim Rejections - 35 USC ' 103*

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. **Claims 1-18** are rejected under 35 U.S.C. 103(a) as being unpatentable over Patterson et al. *("Computer Organization and Design")* and in view of Glew et al. *(US Patent Number 5,751,996)*.

7. As per **Claims 1, 9 and 12**, and more specifically to Claim 12, Patterson discloses

a general purpose computer system *(Macintosh 7200 series, Figure 8.16, page 687)* incorporating at least one CPU *("Processor", Figure 8.16, page 687)* and associated cache *(Figure 7.13, page 561)* in communication with a CPU bus *(line between Processor and PCI interface/memory controller, Figure 8.16, page 687)*, at least one I/O device *(device connected to I/O controller, Figure 8.16, page 687)* and at least one CPU *("Processor", Figure 8.16, page 687)* both in communication with a processor bus *(PCI bus, Figure 8.16, page 687)*, the at least one CPU and associated cache and the at least one I/O device are all in communication with a shared memory *(Main memory, Figure 8.16, page 687)*, the communication provided by a system controller *(PCI interface/memory controller, Figure 8.16, page 687)* having CPU interface logic and I/O interface

logic, a method for processing I/O transactions between the at least one I/O device and the shared memory comprising:

B) programming the CPU interface logic to respond to all addresses that correspond to shared memory *(inherent in the memory controller, in that the controller would not control the memory unless it responded to addresses it contains, Figure 8.16, page 687)*;

E) receiving at the system controller an I/O request from the at least one I/O device *(inherent in the PCI interface/memory controller, in that the PCI interface interfaces with all the devices connected to the PCI bus, including the I/O devices, Figure 8.16, page 687)*; and

Patterson does not disclose the system controller having a plurality of operation modes or the method comprising the steps of A, C, D or F.

Glew discloses a method for processing I/O transactions comprising:

having a plurality of operational modes *(column 7, lines 27-35)*;

A) assigning first *(uncacheable (UC), column 7 lines 28-29)* and second *(write-through cacheable (WT), column 7 lines 32-33)* memory address ranges to the at least one I/O bus *(column 7 lines 35-39)*;

C) programming the CPU cache to only store data corresponding to one of the memory address ranges *(CPU cache only stores data if memory type for a given range is cacheable, column 7, lines 5-7)*;

D) distinguishing *(column 7 lines 13-16)* between the first and the second memory address ranges and to operate in a first mode *(column 7 lines 16-19)* if

the system controller detects an I/O request address corresponding to the first *(uncacheable, see step A) above)* memory address range and to operate in a second mode *(column 7 lines 7-10)* if the system controller detects an I/O request address corresponding to the second *(write-through cacheable, see step A) above)* memory address range;

F) forwarding the I/O request to the shared memory if the system controller is operating in the first mode and to the cache if the system controller is operating in the second mode *(column 7 lines 16-19)*.

Patterson and Glew are analogous art in that they both deal with microprocessor architectures and caching. At the time of the invention it would have been obvious to one with ordinary skill in the art to modify Patterson's system controller to store the memory address range types as described in Glew and to direct I/O requests from the I/O devices directly to the shared memory if they are uncacheable and to send them to the cache if they are, all based on the address range type of the request.

The motivation for doing so would have been that by defining explicit memory types associated with address spaces, memory instructions can be properly and easily be controlled with the memory type to avoid undesirable memory side effects and minimize system bus traffic *(Glew, column 8 lines 28-35)*.

Therefore, it would have been obvious to combine Patterson's system architecture with Glew's memory address range types for the benefit of avoiding undesirable memory side effects and minimizing system bus traffic, to obtain the invention of Claim 1.

The Examiner notes that both Claims 1 and 9 are broader than Claim 12, so as to allow any rejection of Claim 12 to also reject Claims 1 and 9. The Examiner does not intend to unduly narrow the interpretations of Claims 1 or 9.

8. As per **Claims 2 and 13**, Patterson and Glew disclose the method of Claims 1 and 12 respectively, wherein

the first memory address range *(Glew, uncacheable (UC), column 7 lines 28-29)* corresponds to an I/O transaction processed in a non-coherent manner *(a non-coherent manner is interpreted in light of the specification [page 3 lines 15-20] as not involving the cache)* and the second memory address range *(Glew, write-through cacheable (WT), column 7 lines 32-33)* corresponds to an I/O transaction processed in a coherent manner *(a coherent manner is interpreted in light of the specification [page 3 line 21 to page 4 line 8] as involving the cache)*.

9. As per **Claim 3 and 14**. Patterson and Glew disclose the method of Claims 1 and 12 respectively, wherein

the cache is programmed to store data corresponding to the second memory address range *(inherent in write-through cacheable (WT), column 7 lines 32-33)*.

10. As per **Claim 4 and 15**, Patterson and Glew disclose the method of Claims 1 and 12 respectively, wherein

the first and second memory address ranges are different sizes *(Glew, column 5 lines 9-12)*.

11. As per **Claim 5 and 16**, Patterson and Glew disclose the method of Claims 1 and 12 respectively, wherein

the first and second memory address ranges are the same size *(Glew, column 5 lines 12-14)*.

12. As per **Claim 6 and 17**, Patterson and Glew disclose the method of Claims 1 and 12 respectively, wherein

the first operation mode *(Glew, uncacheable (UC), column 7 lines 28-29)* processes the I/O request non-coherently *(see 103 rejections of Claims 2 and 13 above)* and the second operation mode *(Glew, write-through cacheable (WT)* processes the I/O request coherently *(see 103 rejections of Claims 2 and 13 above)*.

13. As per **Claim 7**, Patterson and Glew disclose the method of Claim 1, wherein

the step of programming the system controller includes setting an I/O address decoder on the system controller *(Glew, column 7 lines 36-39)*.

14. As per **Claim 8**, Patterson and Glew disclose the method of Claim 1, wherein

the at least one I/O bus is a processor bus *(PCI bus, Figure 8.16, page 687)*.

15. As per **Claim 10**, Patterson and Glew disclose the method of processing I/O transactions in Claim 9, wherein

the I/O request corresponds to the assigned memory address range *(Glew, column 7 lines 13-27)*.

16. As per **Claim 11**, Patterson and Glew disclose the method of processing I/O transactions in Claim 9, wherein

> the step of setting the system controller includes programming the I/O address decoder so that the memory address range selects the CPU master unit *(Glew, column 7 lines 36-39)*.

17. As per **Claim 18**, Patterson and Glew disclose the method of Claim 12, wherein

> the step of programming the system controller includes setting a PCI target address decoder on the system controller *(Glew, column 7 lines 36-39)*.

## V. RELEVANT ART CITED BY THE EXAMINER

18. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Anderson *(US Patent Numbers 6,651,115 and 6,529,968)* discloses a DMA controller and a memory controller copying data from a non-coherent memory space.

Lau *(US Patent Number 5,485,592)* discloses a cache controller in combination with one or more DMA controllers.

Watkins et al *(US Patent Number 5,263,142)* discloses an I/O cache with mapped pages allocated for caching direct memory access data based on the type of I/O devices.

## VI. CLOSING COMMENTS

### *Conclusion*

#### a. STATUS OF CLAIMS IN THE APPLICATION

19. The following is a summary of the treatment and status of all claims in the application as recommended by M.P.E.P. ' 707.07(i):

#### a(1). CLAIMS REJECTED IN THE APPLICATION

20. Per the instant office action, Claims 1-18 have received a first action on the merits and are subject of a first action non-final.

#### b. DIRECTION OF FUTURE CORRESPONDENCES

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Sam Dillon whose telephone number is 571- 272-8010. The examiner can normally be reached on 8:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Don Sparks can be reached on 571-272-4201. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

***IMPORTANT NOTE***

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Sam Dillon
Examiner
Art Unit 2185

SAD

DONALD SPARKS
SUPERVISORY PATENT EXAMINER